FINAL

Am28F256

256 Kilobit (32 K x 8-Bit)
CMOS 12.0 Volt, Bulk Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - — 70 ns maximum access time
- **CMOS Low power consumption**
  - — 30 mA maximum active current
  - — 100 µA maximum standby current
  - — No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - — 32-pin PDIP
  - — 32-pin PLCC
  - — 32-pin TSOP
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flasherase Electrical Bulk Chip-Erase**
  - — One second typical chip-erase
- **Flashrite Programming**
  - — 10 µs typical byte-program
  - — 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - — Low cost single transistor memory cell
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F256 is a 256 K Flash memory organized as 32 Kbytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F256 is packaged in 32-pin PDIP, PLCC, and TSOP versions. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F256 is erased when shipped from the factory.

The standard Am28F256 offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256 has separate chip enable (CE#) and output enable (OE#) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256 uses a command register to manage this functionality, while maintaining a standard JEDEC Flash Standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256 uses a 12.0V±5% V_{PP} high voltage input to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC} +1 V.

The Am28F256 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F256 is a half a second. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase alrogithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15-20 minutes required for EPROM erasure using ultra-violet light are eliminated.

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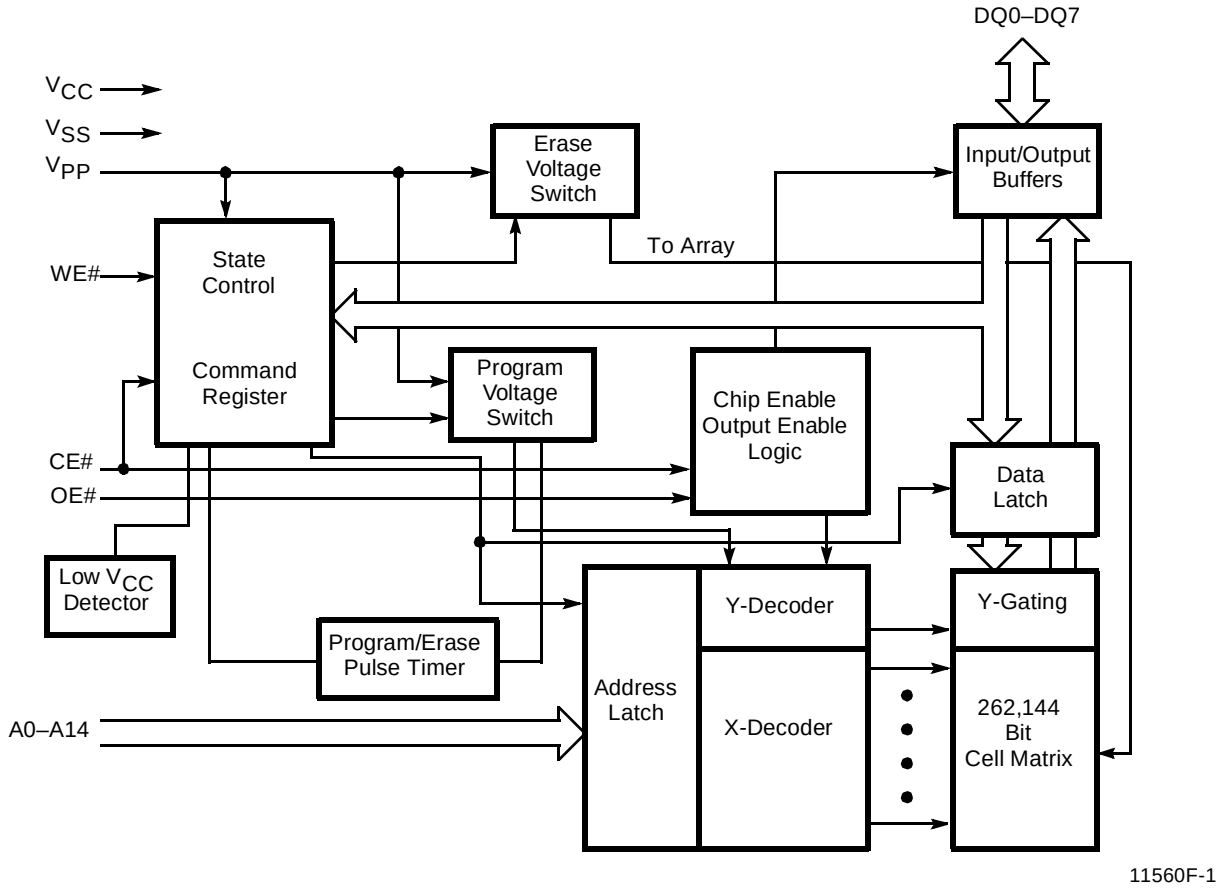
Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256 is designed to support either WE# or CE# controlled writes. During a system write cycle, addresses are latched on the falling edge of WE# or CE# whichever occurs last. Data is latched on the rising edge of WE# or CE# whichever occurs first. To simplify the following discussion, the WE# pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the WE# signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM

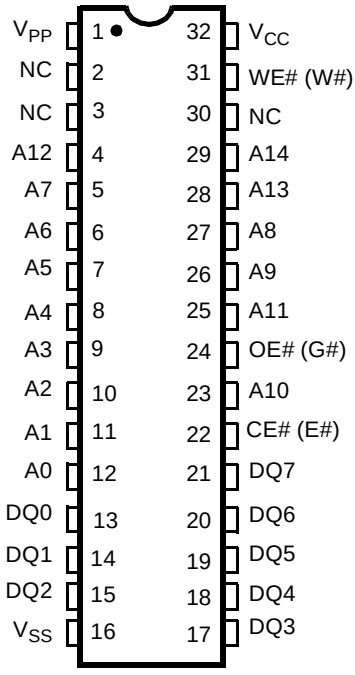


PRODUCT SELECTOR GUIDE

Family Part Number	Am28F256				
Speed Options (V_{CC} = 5.0 V ± 10%)	**-70**	**-90**	**-120**	**-150**	**-200**
Max Access Time (ns)	70	90	120	150	200
CE# (E#) Access (ns)	70	90	120	150	200
OE# (G#) Access (ns)	35	35	50	55	55

CONNECTION DIAGRAMS

PDIP



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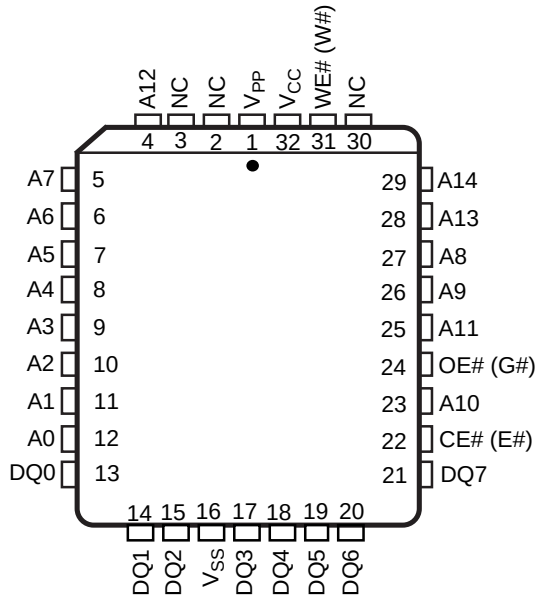
PLCC



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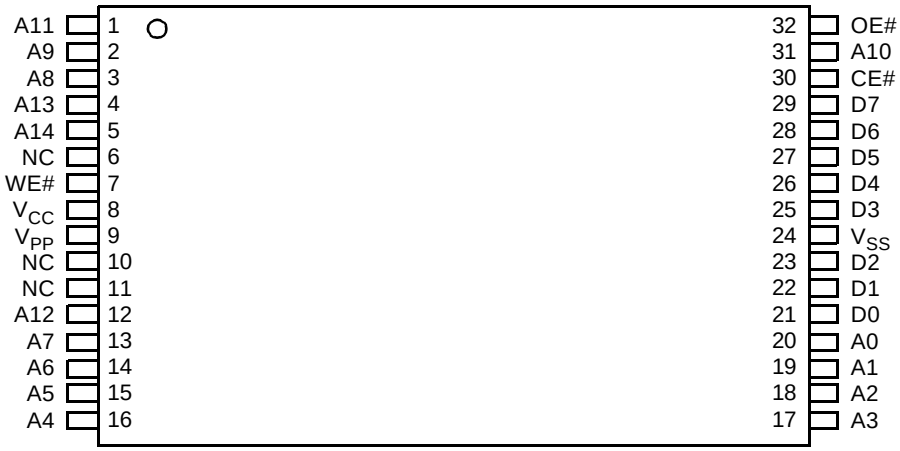
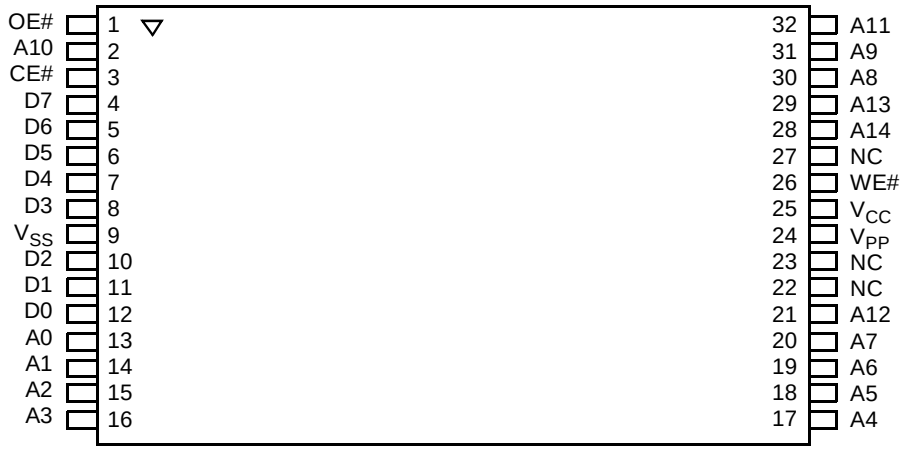
Note: *Pin 1 is marked for orientation.*

CONNECTION DIAGRAMS (continued)



32-Pin TSOP—Standard Pinout



32-Pin TSOP—Reverse Pinout

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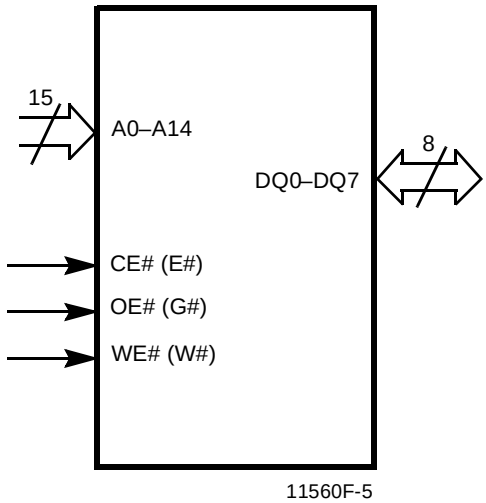
LOGIC SYMBOL



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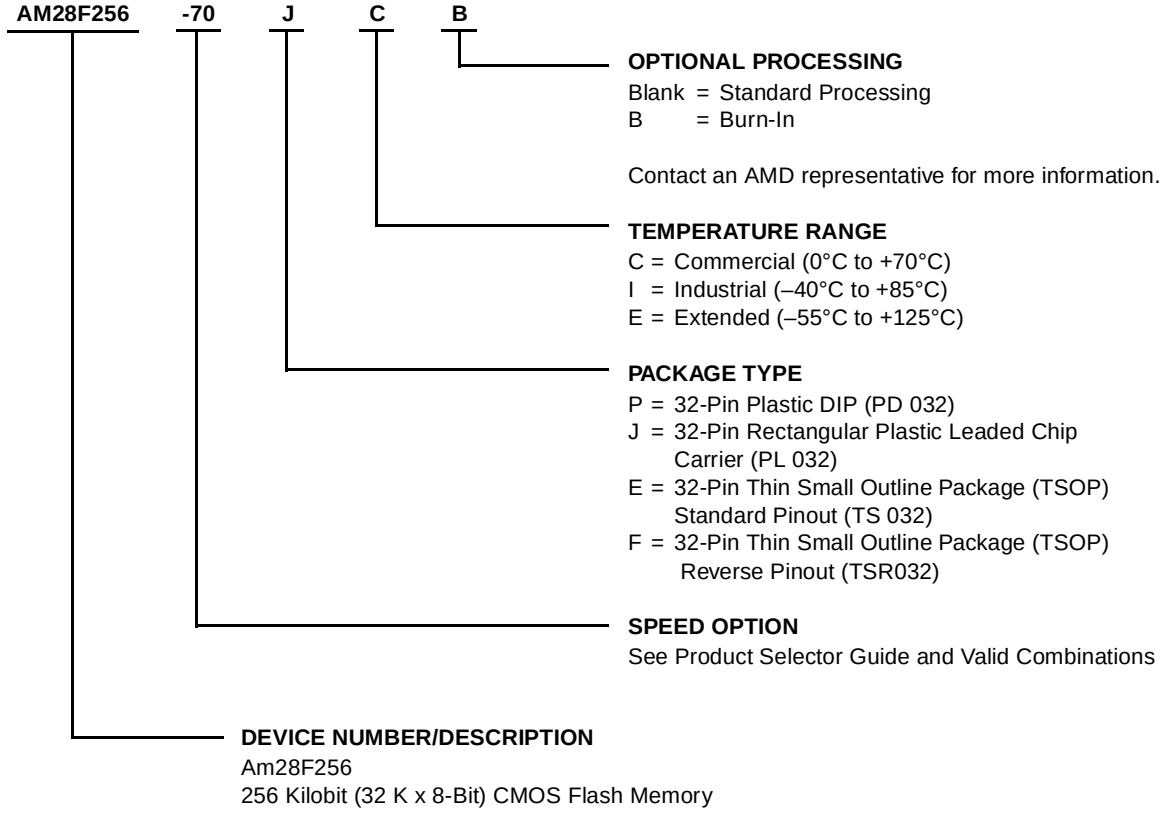
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F256-70	PC, PI, PE, JC, JI, JE, EC, EI, EE, FC, FI, FE
AM28F256-90	
AM28F256-120	
AM28F256-150	
AM28F256-200	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A0–A14

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

CE# (E#)

Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC

No Connect-corresponding pin is not connected internally to the die.

OE# (G#)

Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles. Output Enable is high during command sequencing and program/erase operations.

V_{CC}

Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}

Program voltage input. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}

Ground

WE# (W#)

Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse. Write Enable high inhibits writing to the device.

BASIC PRINCIPLES

The device uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% high voltage input.

Read Only Memory

Without high V_{PP} voltage, the device functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The device's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the device is designed to support either WE# or CE# controlled writes. During a system write cycle, addresses are latched on the falling edge of WE# or CE# whichever occurs last. Data is latched on the rising edge of WE# or CE# whichever occur first. To simplify the following discussion, the WE# pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the WE# signal.

Overview of Erase/Program Operations

Flasherase™ Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note: *The Flash memory array must be completely programmed to 0's prior to erasure. Refer to the Flashrite™ Programming Algorithm.*

1. **Erase Setup:** Write the Setup Erase command to the command register.
2. **Erase:** Write the Erase command (same as Setup Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-Verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFh data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Setup:** Write the Setup Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-Verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified successfully, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. The device powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, the device locks out write cycles for

$V_{CC} < V_{LKO}$ (see DC Characteristics section for voltages). When $V_{CC} < V_{LKO}$, the command register is disabled, all internal program/erase circuits are disabled, and the device resets to the read mode. The device ignores all writes until $V_{CC} > V_{LKO}$. The user must ensure that the control pins are in the correct logic state when $V_{CC} > V_{LKO}$ to prevent uninitentional writes.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on OE#, CE# or WE# will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

Power-up of the device with WE# = CE# = V_{IL} and OE# = V_{IH} will not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F256 Device Bus Operations (Notes 7 and 8)

Operation		CE# (E#)	OE# (G#)	WE# (W#)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01h)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A1h)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels. $V_{PPL} = V_{PP} < V_{CC} + 2$ V. See DC Characteristics for voltage levels of V_{PPH}. 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} + 2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *11.5 < V_{ID} < 13.0 V. Minimum V_{ID} rise time and fall time (between 0 and V_{ID} voltages) is 500 ns.*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.*
8. *If $V_{CC} \leq$ 1.0 Volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 volts. Also, the Am28F256 has a V_{PP} rise time and fall time specification of 500 ns minimum.*

READ ONLY MODE

When V_{PP} is less than V_{CC} + 2 V, the command register is inactive. The device can either read array or autoselect data, or be standby mode.

Read

The device functions as a read only memory when V_{PP} < V_{CC} + 2 V. The device has two control functions. Both must be satisfied in order to output data. CE# controls power to the device. This pin should be used for specific device selection. OE# controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable CE# to valid data at the output pins. The output enable access time is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable at least t_{ACC}–t_{OE}).

Standby Mode

The device has two standby modes. The CMOS standby mode (CE# input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode (CE# is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the OE# input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when OE# is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0 V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the device these two bytes are given in Table 2 below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

Table 2. Am28F256 Auto Select Code

Type	A0	Code (HEX)
Manufacturer Code	V_{IL}	01
Device Code	V_{IH}	A1

ERASE, PROGRAM, AND READ MODE

When V_{PP} is equal to 12.0 V ± 5%, the command register is active. All functions are available. That is, the device can program, erase, read array or autoselect data, or be standby mode.

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing WE# and CE# to V_{IL}, while OE# is at V_{IH}. Addresses are latched on the falling edge of WE#, while data is latched on the rising edge of the WE# pulse. Standard microprocessor write timings are used.

The device requires the OE# pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, OE# must be V_{IH}, and CE# and WE# must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00h (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00h into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00h (read mode) upon V_{PP} power-up. The 00h (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F256 Command Definitions

Command (Note 4)	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory	Write	X	00h/FFh	Read	RA	RD
Read Auto select	Write	X	80h or 90h	Read	00h/01h	01h/A1h
Erase Set-up/Erase Write	Write	X	20h	Write	X	20h
Erase-Verify	Write	EA	A0h	Read	X	EVD
Program Setup/Program	Write	X	40h	Write	PA	PD
Program-Verify	Write	X	C0h	Read	X	PVD
Reset	Write	X	FFh	Write	X	FFh

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   X = Don't care.
   Addresses are latched on the falling edge of the WE# pulse.
3. *RD = Data read from location RA during read operation.*
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of WE#.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. *Refer to the appropriate section for algorithms and timing diagrams.*

FLASHERASE ERASE SEQUENCE

Erase Setup

Erase Setup is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20h is written to the command register in order to perform the Erase Setup operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20h) again to the register. The erase operation begins with the rising edge of the WE# pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Setup and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note: *The Flash memory device must be fully programmed to 00h data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.*

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0h to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the WE# pulse or CE# pulse, whichever occurs later. The rising edge of the WE# pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the device applies an internally generated margin voltage to the addressed byte. Reading FFh from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of WE# or CE# pulse, whichever occurs later. The process continues for each byte in the memory array until a byte does not return FFh data or all the bytes in the array are accessed and verified.

If an address is not verified to FFh data, the entire chip is erased again (refer to Erase Setup/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program Setup) to the command register. Figure 1 and Table 4, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

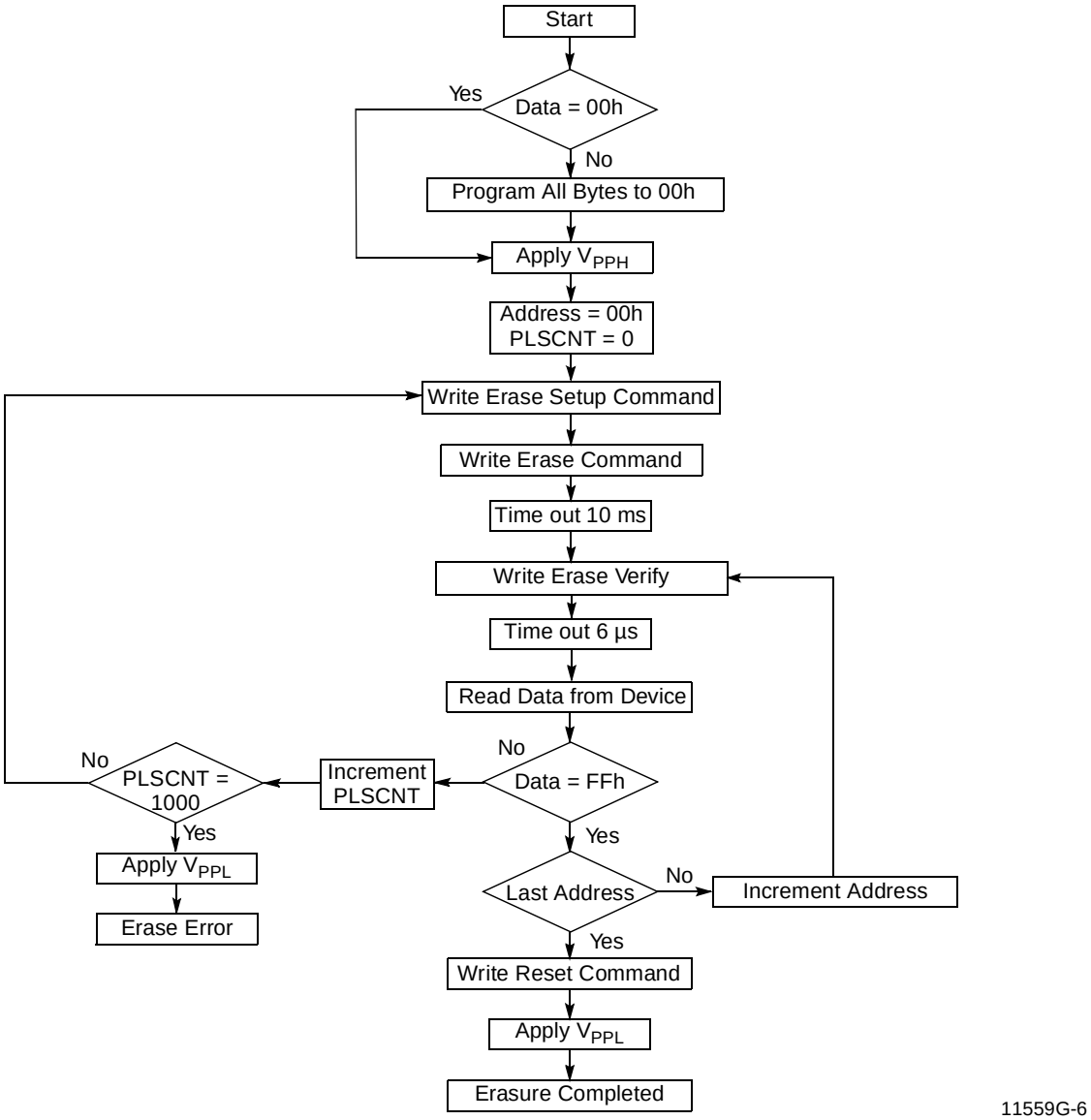


Figure 1. Flasherase Electrical Erase Algorithm

FLASHERASE ELECTRICAL ERASE ALGORITHM

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The device is erased when shipped from the factory. Reading FFh data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

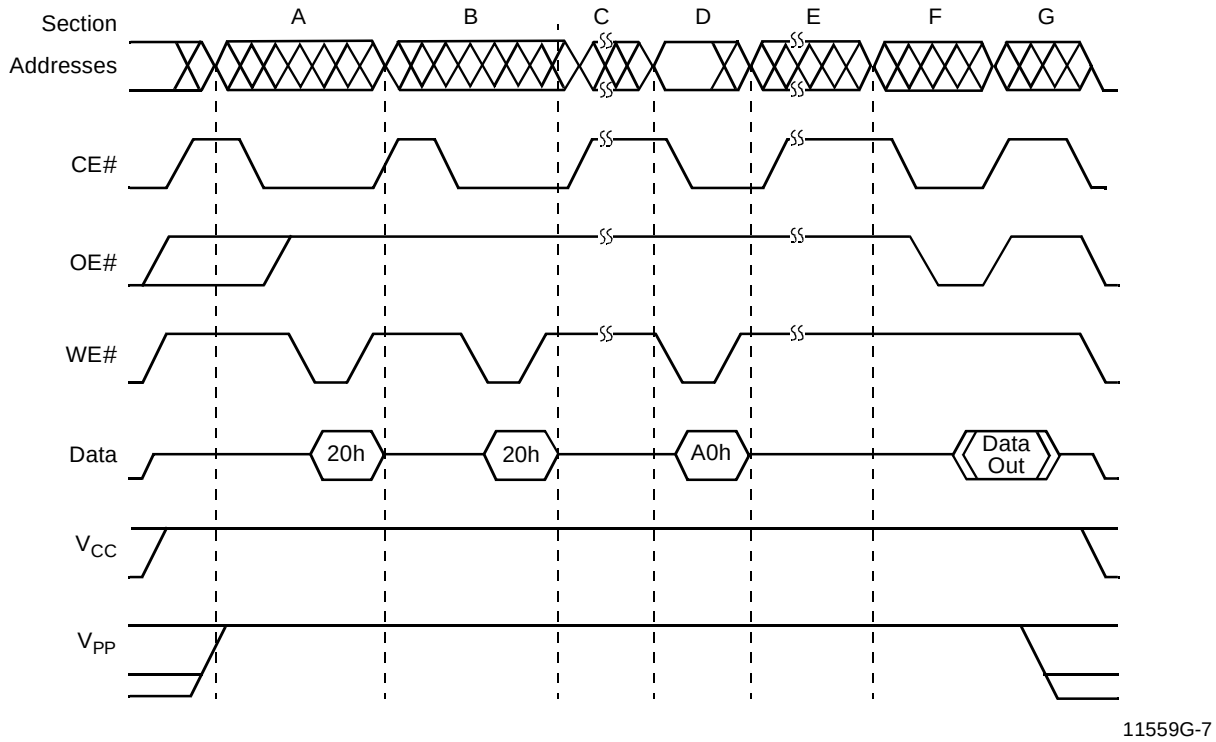
Should the device be currently programmed, data other than FFh will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00h). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFh) begins at address 0000h and continues through the array to the last address, or until data other than FFh is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (one second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase pulses are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 4. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00h before erasure (Note 3) ***Note:*** *Use Flashrite programming algorithm (Figure 3) for programming.*
Standby		Wait for V_{PP} Ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Setup	Data = 20h
	Erase	Data = 20h
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0h Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFh Increment pulse count
Write	Reset	Data = FFh, reset the register for read operations
Standby		Wait for V_{PP} Ramp to V_{PPL} (Note 1)

Notes:

1. *See AC and DC Characteristics for values of V_{PP} parameters. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.*
3. *The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	20h	20h	N/A	A0h	N/A	Compare Data	N/A
Function	Erase Setup	Erase	Erase (10 ms)	Erase-Verify	Transition (6 µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. AC Waveforms For Erase Operations

ANALYSIS OF ERASE TIMING WAVEFORM

Note: *This analysis does not include the requirement to program the entire array to 00h data prior to erasure. Refer to the Flashrite Programming algorithm.*

Erase Setup/Erase

This analysis illustrates the use of two-cycle erase commands (section A and B). The first erase command (20h) is a Setup command and does not affect the array data (section A). The second erase command (20h) initiates the erase operation (section B) on the rising edge of this WE# pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the WE# pulse of section B.

Note: *An integrated stop timer prevents any possibility of overerasure by limiting each time-out period of 10 ms.*

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0h). This command terminates the erase operation on the rising edge of the WE# pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with

the Erase-verify command (section D). Addresses are latched on the falling edge of the WE# pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFh data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFh data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Note: *All address locations must be programmed to 00h prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.*

FLASHRITE PROGRAMMING SEQUENCE

Program Setup

The device is programmed byte by byte. Bytes may be programmed sequentially or at random. Program Setup is the first of a two-cycle program command. It stages the device for byte programming. The Program Setup operation is performed by writing 40h to the command register.

Program

Only after the program Setup operation is completed will the next WE# pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second WE# pulse. Addresses and data are internally latched on the falling and rising edge of the WE# pulse respectively. The rising edge of WE# also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Setup and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0h into the command register in order to initiate the Program-verify operation. The rising edge of this WE pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the device applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Program Setup/Program). Figure 3 and Table 5 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The device Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 µs programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 5 illustrate the programming algorithm.

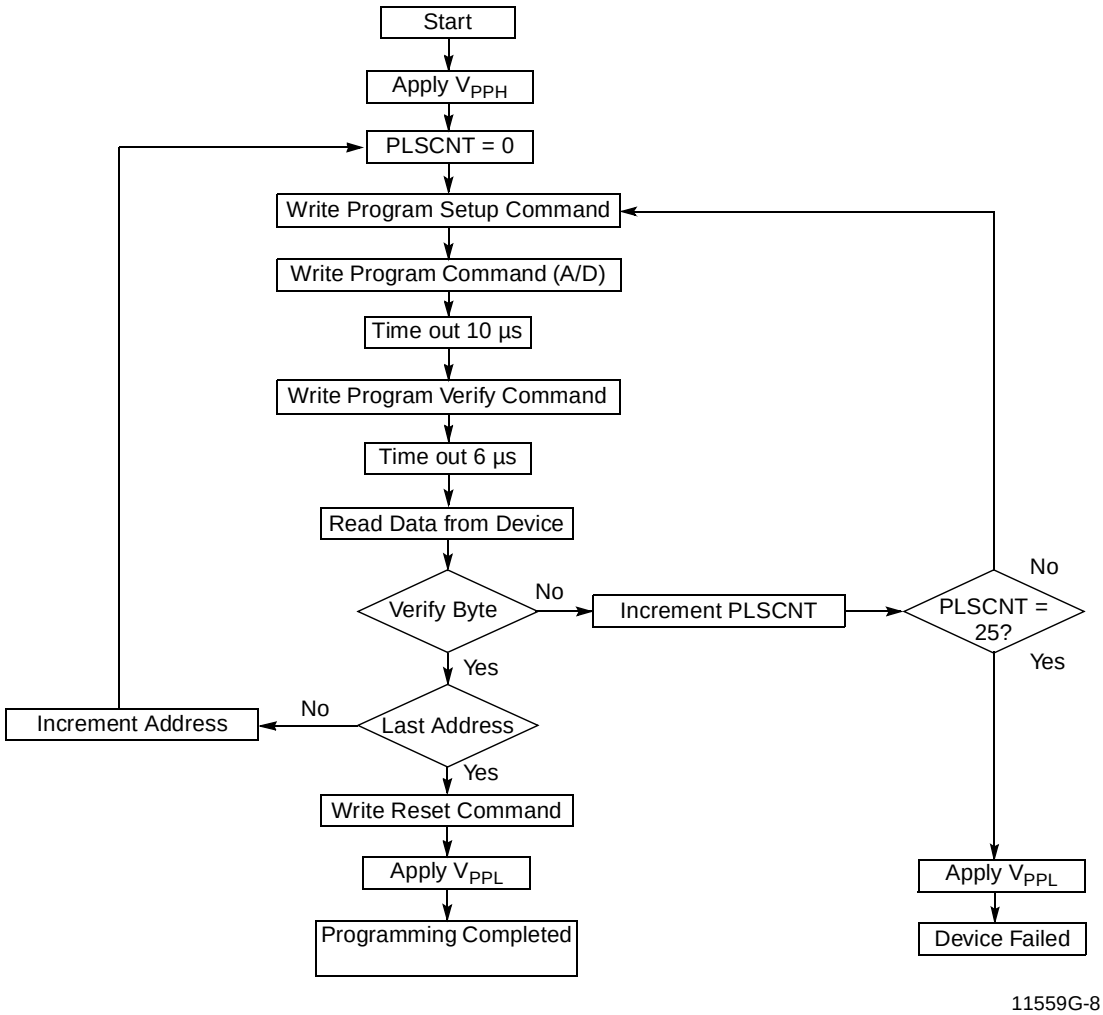


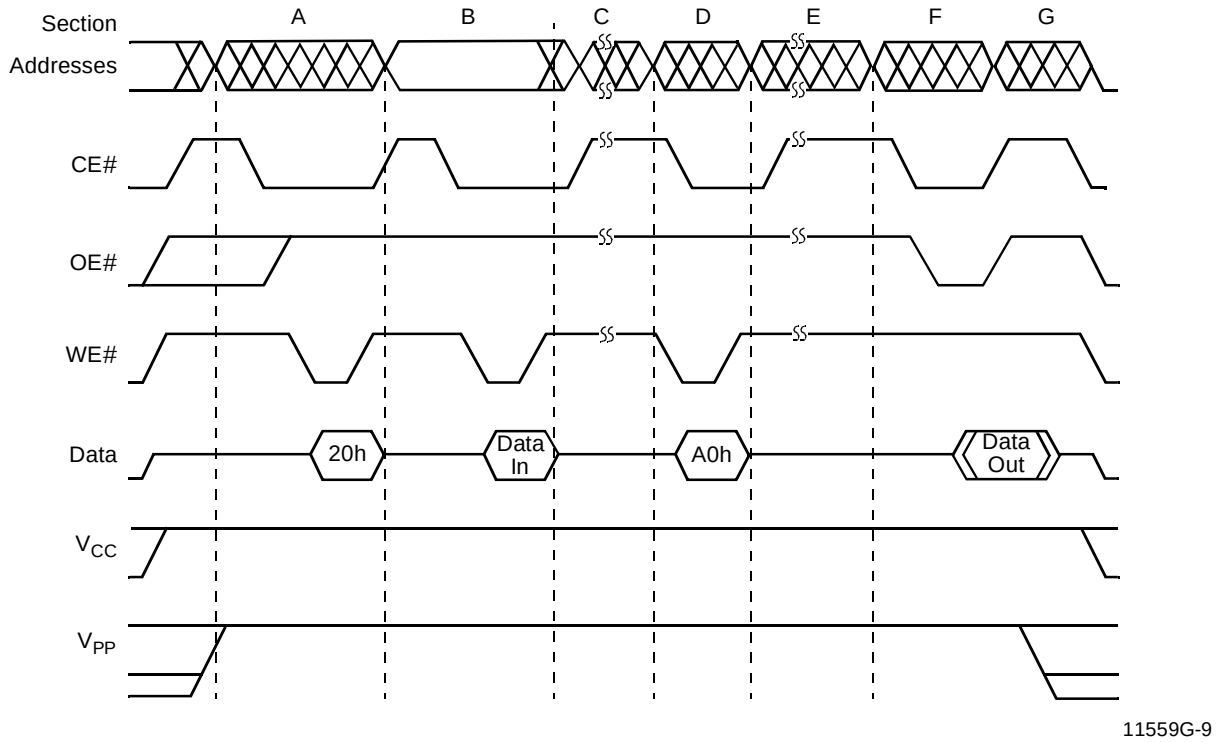
Figure 3. Flashrite Programming Algorithm

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (Note 1) Initialize Pulse counter
Write	Program Setup	Data = 40h
	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (Note 2)	Data = C0h Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Reset	Data = FFh, resets the register for read operations.
Standby		Wait for V_{PP} Ramp to V_{PPL} (Note 1)

Notes:

1. *See AC and DC Characteristics for values of V_{PP} parameters. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	40h	Program Address, Program Data	N/A	C0h (Stops Program)	N/A	Compare Data	N/A
Function	Program Setup	Program Command Latch Address and Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. AC Waveforms for Programming Operations

ANALYSIS OF PROGRAM TIMING WAVEFORMS

Program Setup/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40h) is a Setup command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of WE# respectively (section B). The rising edge of this WE# pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the WE# pulse of section B.

Note: *An integrated stop timer prevents any possibility of overprogramming by limiting each time-out period of 10 µs.*

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0h). This command terminates the programming operation on the rising edge of the WE# pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for

generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP} the delay required is proportional to the number of devices being erased and the 0.1 mF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse.
3. A third delay time is required for each programming pulse width (10 ms). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 ms). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note: *Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.*

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00h).

Power-Up/Power-Down Sequence

The device powers-up in the Read only mode. Power supply sequencing is not required. Note that if $V_{CC} \leq$ 1.0 Volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 Volts. Also, the device has V_{PP} rise time and fall time specification of 500 ns minimum.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the setup Program command (40h). This will reset the device to the Read mode.

Following any other Flash command write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Setup Program command (40h) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFh data is considered null data during programming operations (memory cells are only programmed from a logical “1” to “0”). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the setup Program state or not.

Programming In-System

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The device contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80h or 90h into the command register. Following this command, a read cycle address 0000h retrieves the manufacturer code of 01h. A read cycle from address 0001h returns the device code. To terminate the operation, it is necessary to write another valid command, such as Reset (FFh), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Plastic Packages . . . . . –65°C to +125°C

Ambient Temperature
with Power Applied. . . . . .–55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP} (Note 1) .–2.0 V to +7.0 V

V_{CC} (Note 1). . . . . .–2.0 V to +7.0 V

A9 (Note 2). . . . . .–2.0 V to +14.0 V

V_{PP} (Note 2). . . . . .–2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.0 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A). . . . . .0°C to +70°C

Industrial (I) Devices
Ambient Temperature (T_A). . . . . .–40°C to +85°C

Extended (E) Devices
Ambient Temperature (T_A). . . . . .–55°C to +125°C

V_{CC} Supply Voltages
V_{CC} . . . . . +4.50 V to +5.50 V

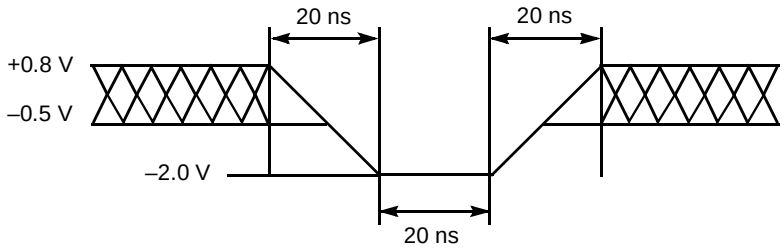
V_{PP} Voltages
Read . . . . . –0.5 V to +12.6 V

Program, Erase, and Verify . . . . . +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

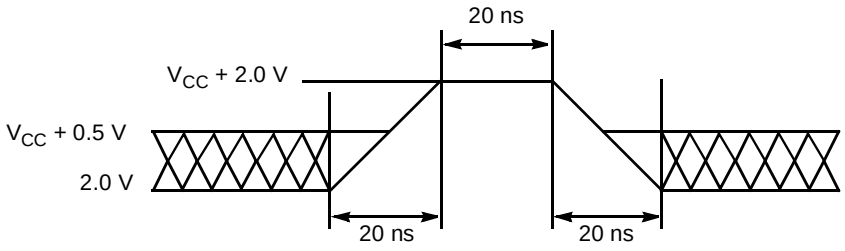
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



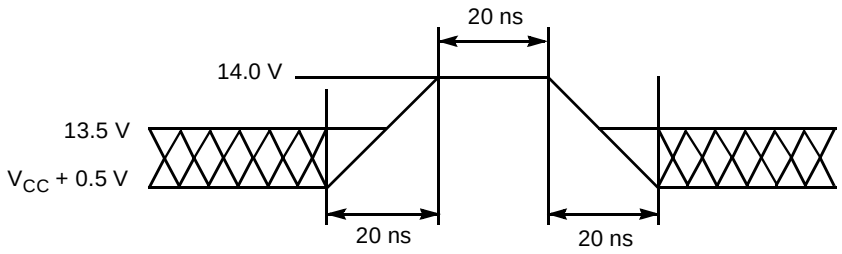
11560F-10

Maximum Positive Input Overshoot



11560F-11

Maximum V_{PP} Overshoot



11560F-12

DC CHARACTERISTICS over operating range unless otherwise specified

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, CE# = V_{IL}, OE# = V_{IH} I_{OUT} = 0 mA, at 6 MHz		20	30	mA
I_{CC2}	V_{CC} Programming Current	CE# = V_{IL} Programming in Progress (Note 4)		20	30	mA
I_{CC3}	V_{CC} Erase Current	CE# = V_{IL} Erasure in Progress (Note 4)		20	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max, $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	3.7		V

Notes:

1. ***Caution:*** *The Am28F256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied. If $V_{CC} \leq 1.0$ Volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 Volts. Also, the Am28F256 has a V_{PP} rise time and fall time specification of 500 ns minimum.*
2. *I_{CC1} is tested with OE# = V_{IH} to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# = V_{CC} + 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, CE# = V_{IL}, OE# = V_{IH} I_{OUT} = 0 mA, at 6 MHz		20	30	mA
I_{CC2}	V_{CC} Programming Current	CE# = V_{IL} Programming in Progress (Note 4)		20	30	mA
I_{CC3}	V_{CC} Erase Current	CE# = V_{IL} Erasure in Progress (Note 4)		20	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max, $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PPL} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	3.7		V

Notes:

1. ***Caution:*** *The Am28F256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied. If $V_{CC} \leq 1.0$ volt, the voltage difference between V_{PP} and V_{CC} should not exceed 10.0 volts. Also, the Am28F256 has a V_{PP} rise time and fall time specification of 500 ns minimum.*
2. *I_{CC1} is tested with OE# = V_{IH} to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}*
4. *Not 100% tested.*

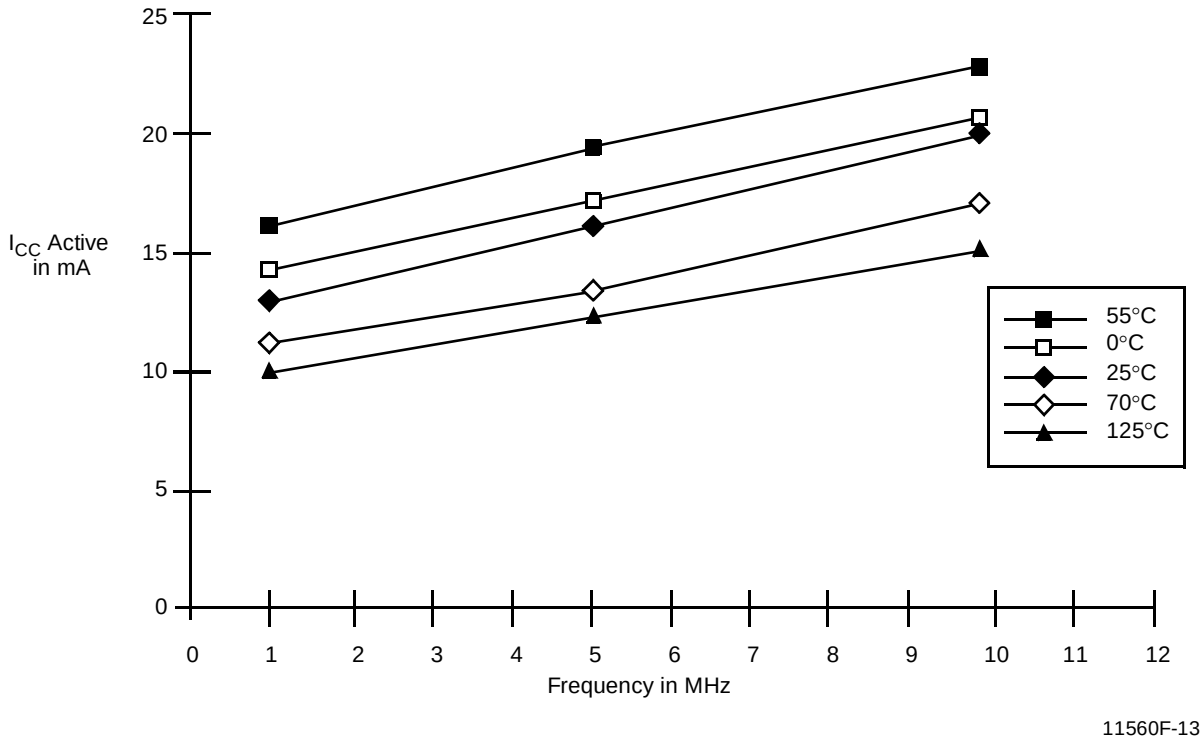
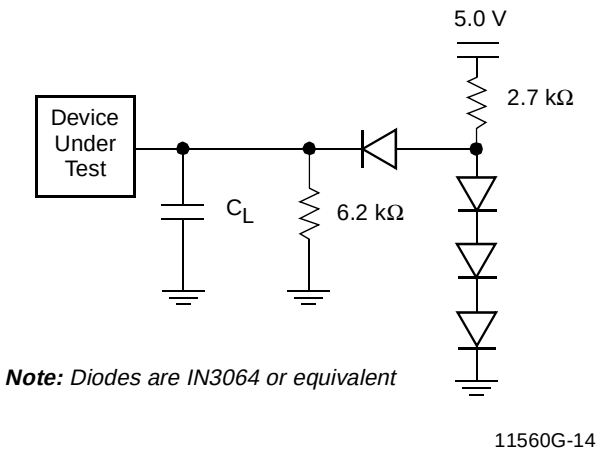


Figure 5. Am28F256—Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

TEST CONDITIONS



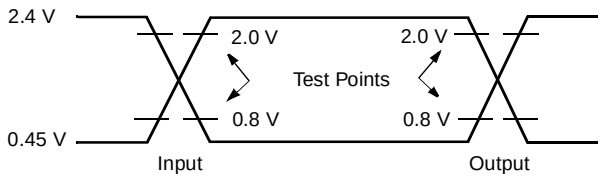
Note: *Diodes are IN3064 or equivalent*

Figure 6. Test Setup

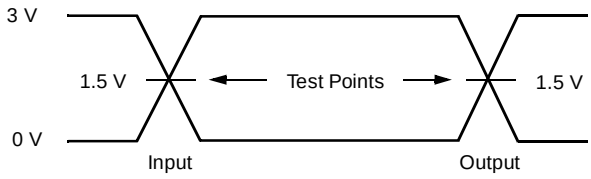
Table 6. Test Specifications

Test Condition	-70	All others	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	≤10		ns
Input Pulse Levels	0.0–3.0	0.45–2.4	V
Input timing measurement reference levels	1.5	0.8, 2.0	V
Output timing measurement reference levels	1.5	0.8, 2.0	V

SWITCHING TEST WAVEFORMS



AC Testing (all speed options except -70): Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤10 ns.



AC Testing for -70 devices: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤10 ns.

11560G-15

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC Characteristics—Read Only Operation

Parameter Symbols		Parameter Description		Am28F256 Speed Options					Unit
JEDEC	Standard			-70	-90	-120	-150	-200	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 2)	Min	70	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable AccessTime	Max	70	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Max	70	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Max	35	35	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 2)	Min	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 1)	Max	20	20	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 2)	Min	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 2)	Max	20	20	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, CE#, or OE# Change (Note 2)	Min	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min	6	6	6	6	6	µs
t_{VCS}		V_{CC} Setup Time to Valid Read (Note 2)	Min	50	50	50	50	50	µs

Notes:

1. *Guaranteed by design not tested.*
2. *Not 100% tested.*

AC Characteristics—Write/Erase/Program Operations

Parameter Symbols		Parameter Description		Am28F256 Speed Options					Unit
JEDEC	Standard			-70	-90	-120	-150	-200	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 4)	Min	70	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-up Time	Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-up Time	Min	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	45	45	50	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 2)	Min	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation (Note 2)	Min	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Setup Time to Chip Enable LOW (Note 4)	Min	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-up Time to Chip Enable LOW (Note 4)	Min	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 4)	Min	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 4)	Min	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 4)	Min	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *Maximum pulse widths not required because the on-chip program/erase stop timer will terminate the pulse widths internally on the device.*
3. *Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all setup, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.*
4. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

SWITCHING WAVEFORMS

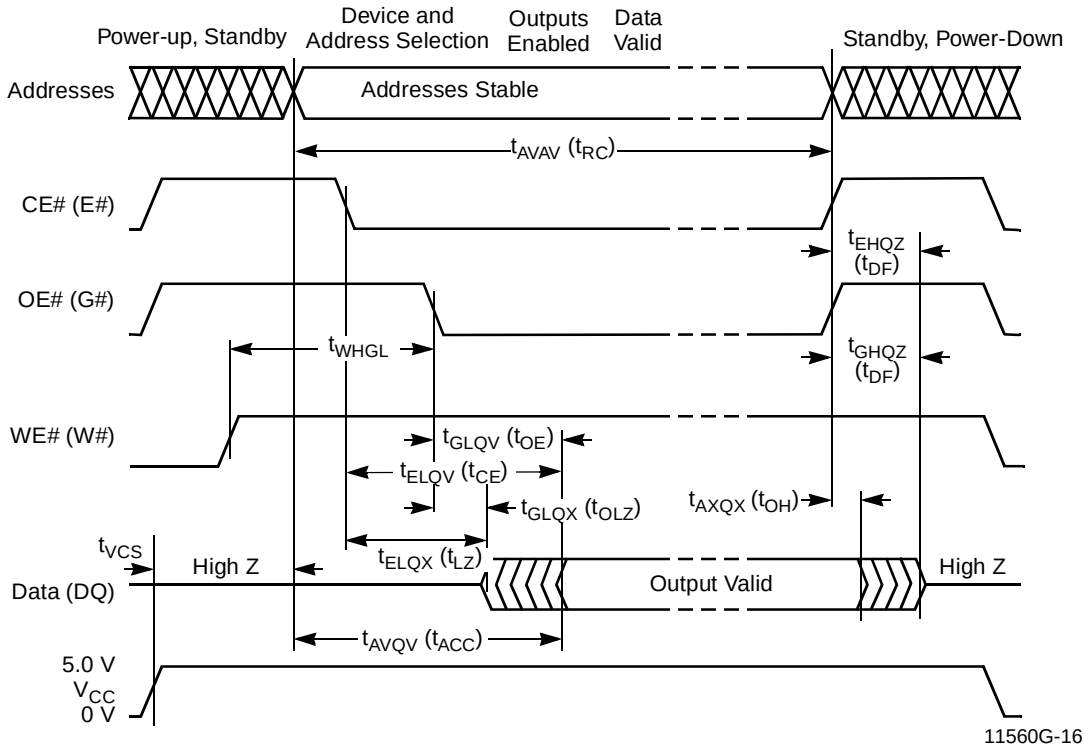


Figure 7. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

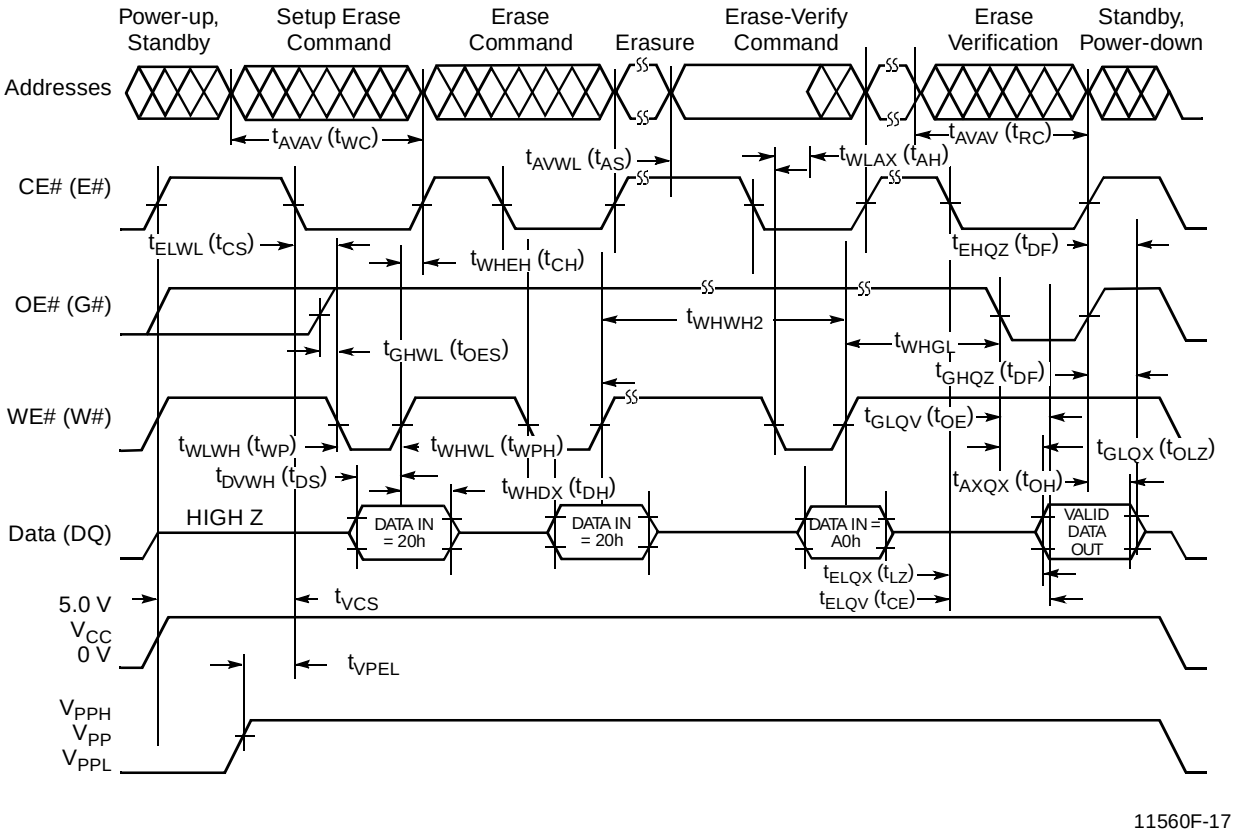


Figure 8. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

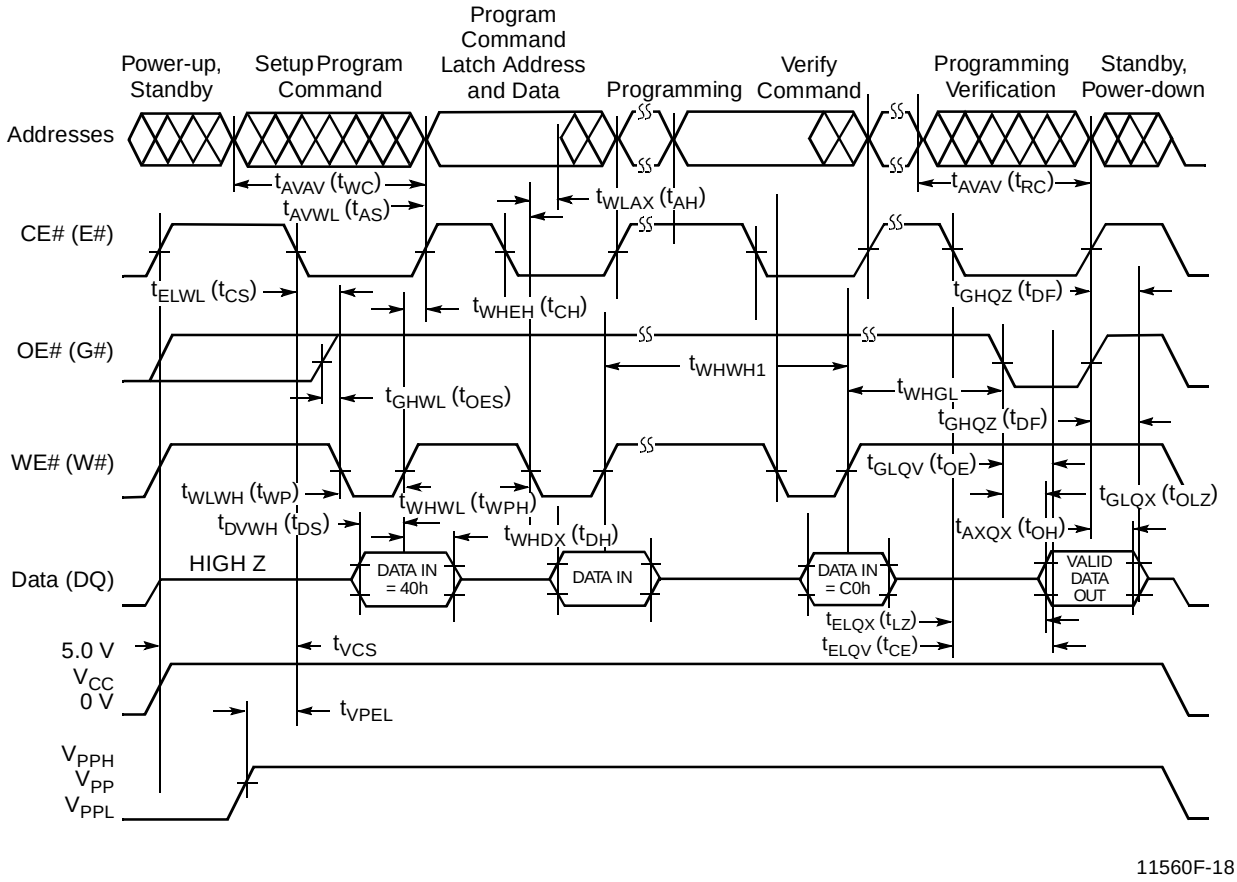


Figure 9. AC Waveforms for Programming Operations

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits				Comments
	Min	Typ (Note 1)	Max (Note 2)	Unit	
Chip Erase Time		1	10	sec	Excludes 00h programming prior to erasure
Chip Programming Time		0.5	3	sec	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. *25°C, 12 V V_{PP}*
2. *Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max and Flashrite = 25 max). Typical worst case for program and erase is significantly less than the actual device limit.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

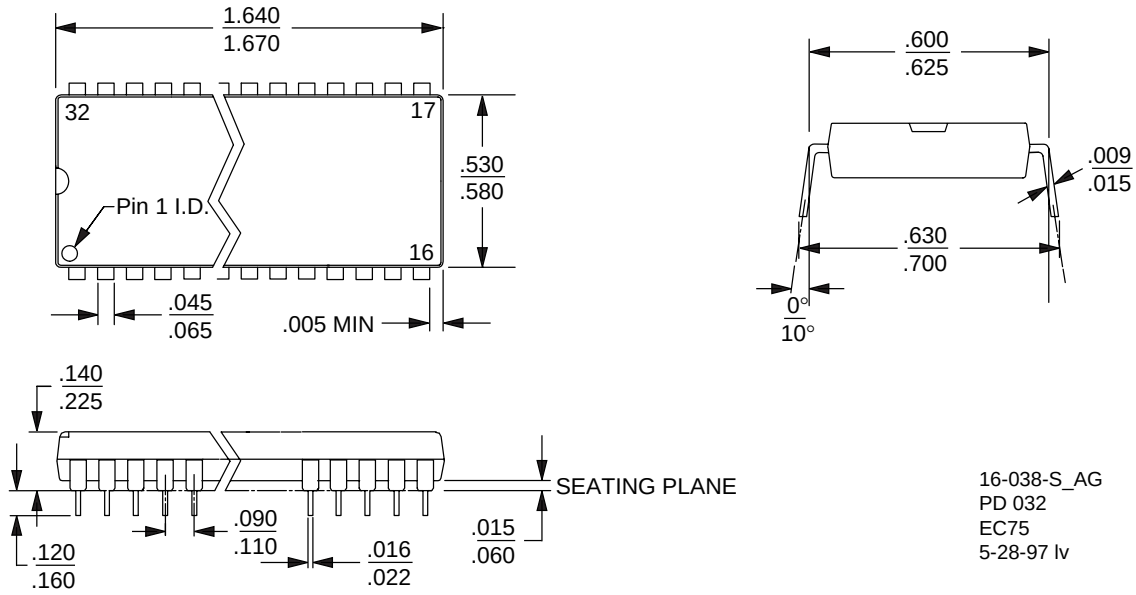
Note: *Sampled, not 100% tested. Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

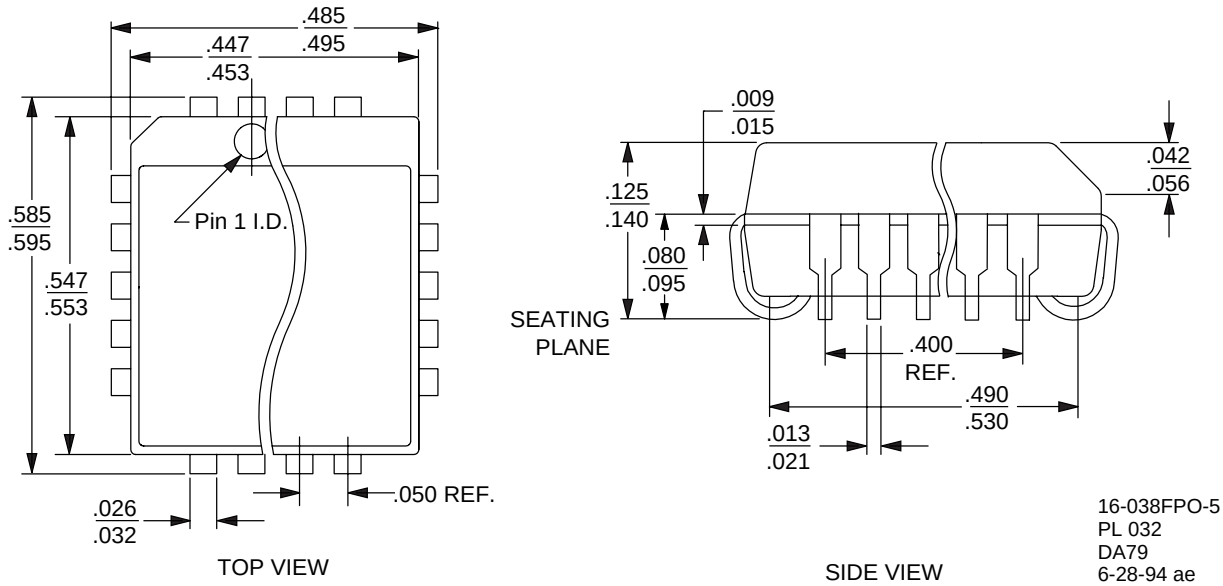
PHYSICAL DIMENSIONS

PD032—32-Pin Plastic DIP (measured in inches)



16-038-S_AG
PD 032
EC75
5-28-97 lv

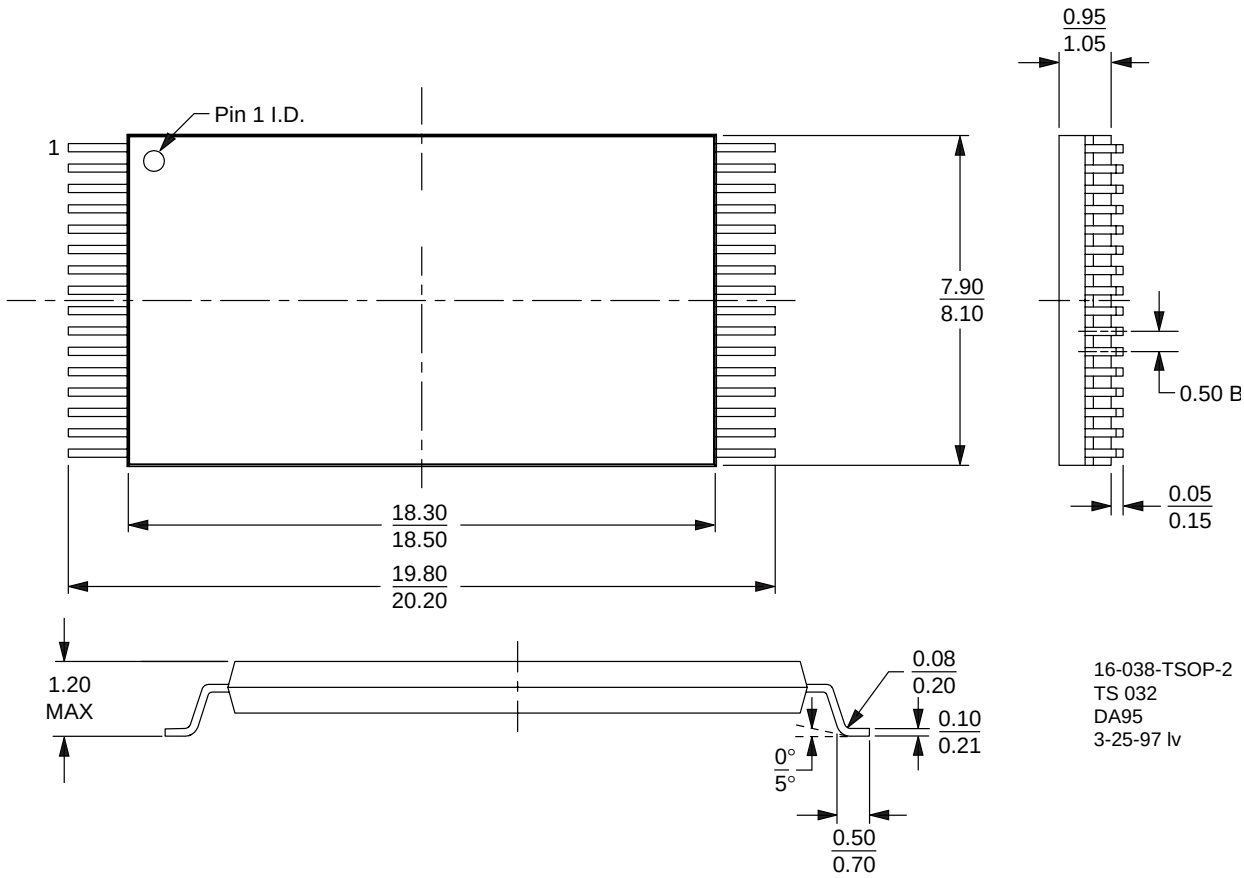
PL032—32-Pin Plastic Leaded Chip Carrier (measured in inches)



16-038FPO-5
PL 032
DA79
6-28-94 ae

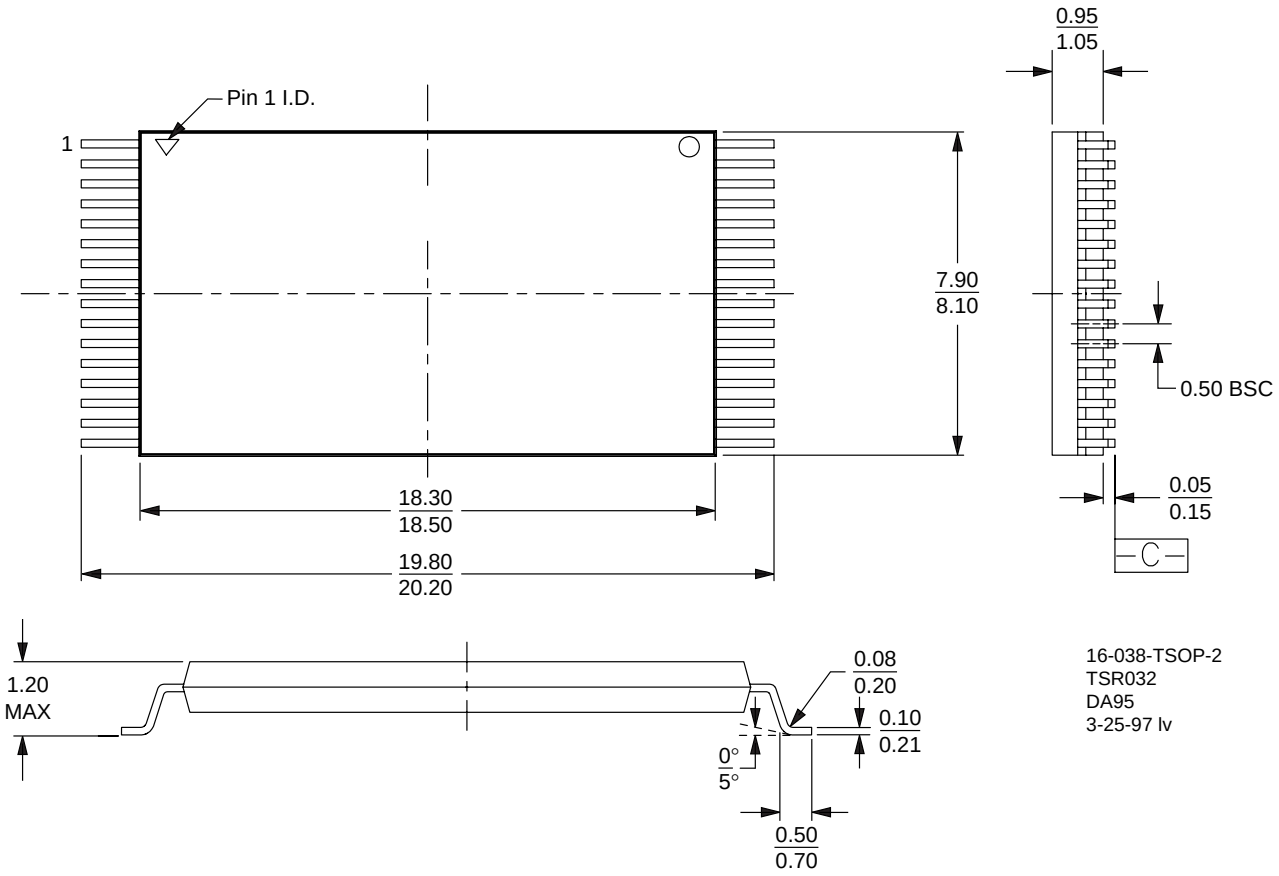
PHYSICAL DIMENSIONS

TS032—32-Pin Standard Thin Small Outline Package (measured in millimeters)



PHYSICAL DIMENSIONS

TSR032—32-Pin Reversed Thin Small Outline Package (measured in millimeters)



DATA SHEET REVISION SUMMARY FOR AM28F256

Revision G

Deleted -75, -95, and -250 speed options. Matched formatting to other current data sheets.

Revision G+1

Figure 3, Flashrite Programming Algorithm: Moved end of arrow originating from Increment Address box so that it points to the PLSCNT = 0 box, not the Write Program Verify Command box. This is a correction to the diagram on page 6-189 of the 1998 Flash Memory Data Book.

Revision G+2

Programming In A PROM Programmer:

Deleted the paragraph "(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system)."

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